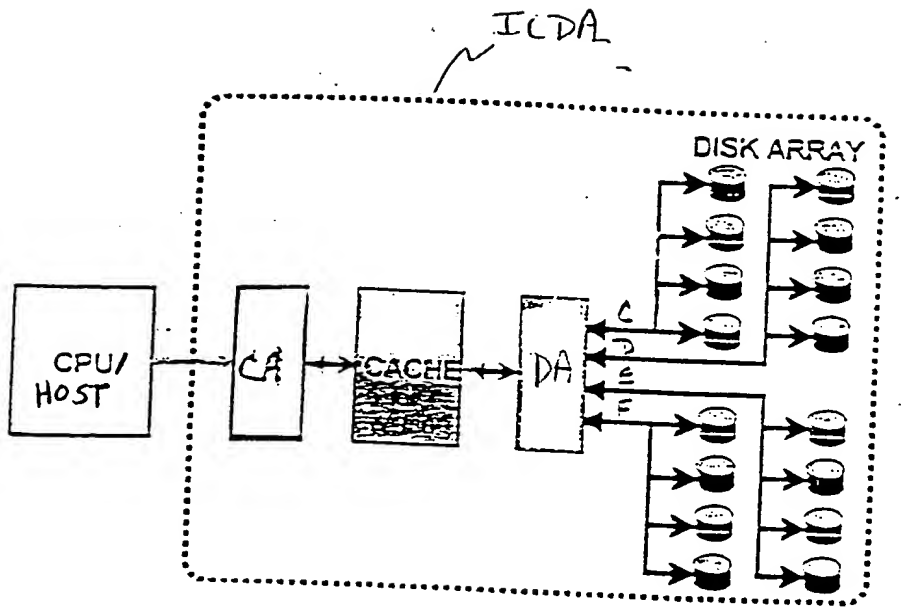
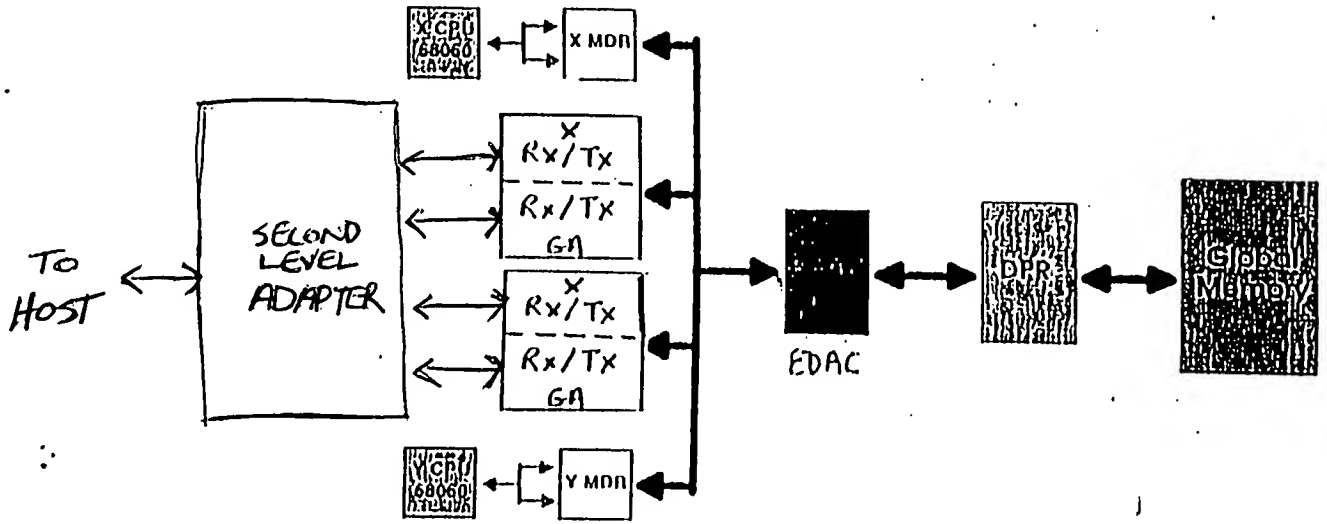


Fig. 1
(prior art)

ESCON FRONT END
(prior art)



Fg 2

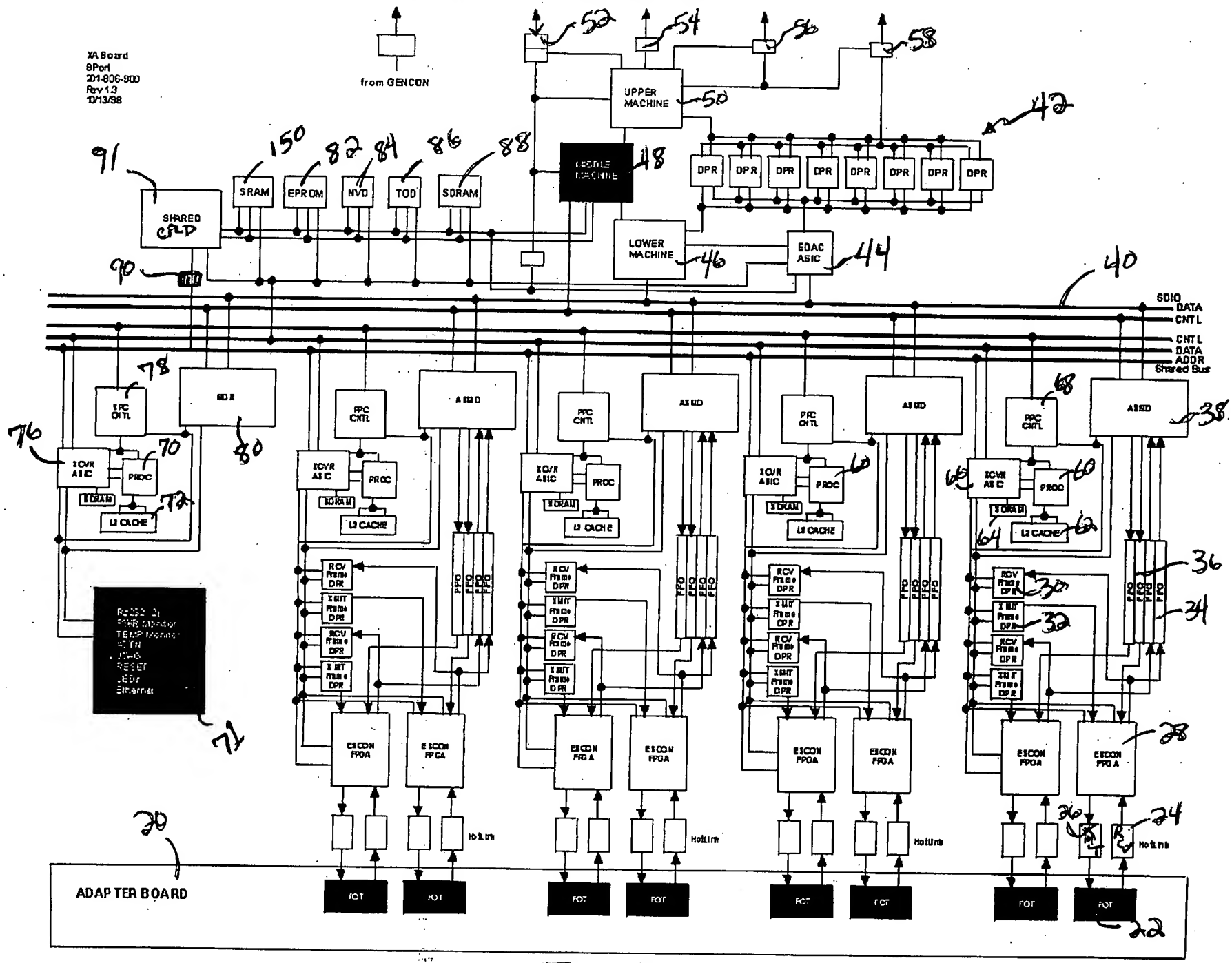
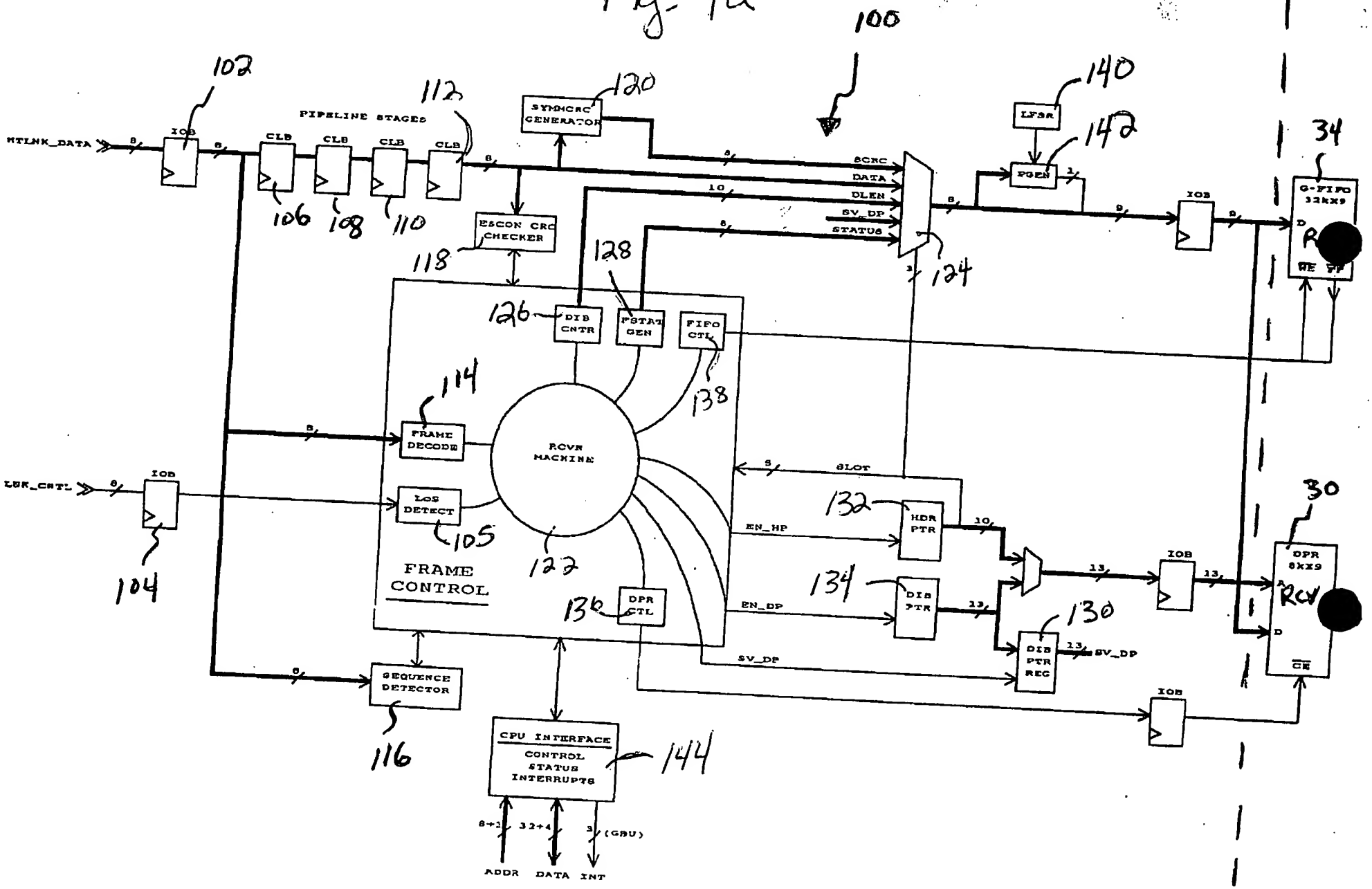

XA Board
8Port
201-806-900
Rev 1.3
10/13/98
from GENCON
UPPER MACHINE
LOWER MACHINE
EDAC ASIC
SHARED CPLD
SRAM
EPROM
NVD
TOD
SDRAM
DPR
SDIO DATA
CNTL
CNTL
DATA
ADDR
Shared Bus
PPC CNTL
ASIC
XCVR ASIC
PROC
L2 CACHE
RCV Frame DPR
XMIT Frame DPR
FIFO
ESCON FPGA
Hotlink
FOT
ADAPTER BOARD

Fig. 3

Fig. 4a



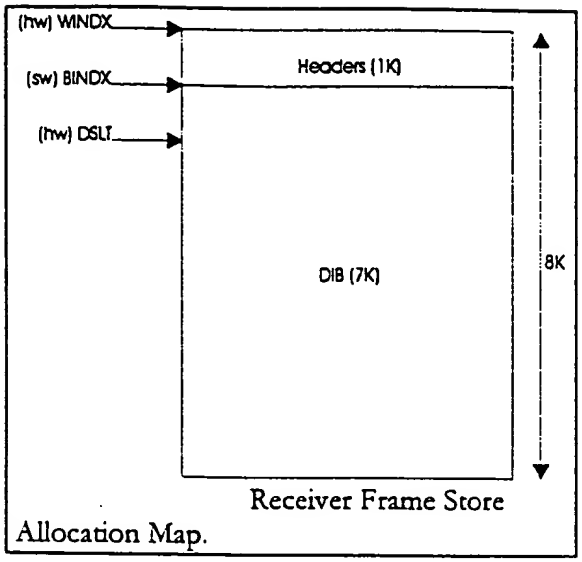


Fig. 4b

	0	7	8	15
0	Data Adr			DSLT
1	Data Len			
2	FStatus		SCRC	
3	Dest Link Addr		0000	Dest Log Adr
4	Src Link Addr		0000	Src Log Adr
5	Link Control		IFI	
6	Device Adr 0		Device Adr 1	
7	DHF		XX	

Device Frame
Header Structure.

Fig. 4c

	0	7	8	15
0	Data Adr			DSLT
1	Data Len			
2	FStatus		XX	
3	Dest Link Addr		0000	Dest Log Adr
4	Src Link Addr		0000	Src Log Adr
5	Link Control		XX	

Link Frame Header
Structure.

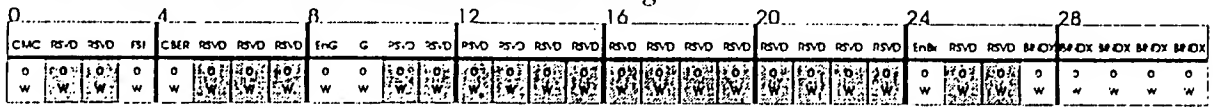
Fig. 4d

TABLE I

Mnemonic	Size	Description
Data Adr	16b	FrameStore Location of data (DIB) portion of frame. If Data Addr=0x0000, DIB is in G-FIFO.
DSLT	3b	DSLT is actually the 3 low-order bits of Data Addr. If DSLT=0x0, the DIB is in G-FIFO. If DSLT=0x1 thru 0x7, the DIB is in the corresponding FrameStore slot.
Data Len	11b	Length of data (DIB) portion of frame. Does not include frame header or Escon CRC.
FStatus	8b	Bits 0–3: ERROR; 4: Full; 5: 0; 6: EOF; 7: SOF **ERROR:** 0000 = No Error 0001 = CRC Error 0010 = Control character received in frame 0011 = Invalid character received in frame 0100 = Maximum size of frame exceeded 0101 = Frame reception ended by 2 IDLE characters 0110 = Frame reception ended by ABORT delimiter 0111 = Frame reception ended by Invalid EOF delimiter *The following errors cause Frame Reception to stop* 1000 = Frame reception ended by LOS detection 1001 = Frame reception ended by Sequence detection 1010 = Frame reception ended by SOF delimiter 1100 = Frame reception ended by G-FIFO overflow **Full:** 1=This frame caused the FrameStore header section to become Full. **EOF:** 0=PEOF detected; 1=DEOF detected **SOF:** 0=PSOF detected; 1=CSOF detected
SCRC	8b	CRC covering DIB of received frame. Only valid for Device-frames independent of whether the DIB goes to FrameStore or G-FIFO.

TABLE II

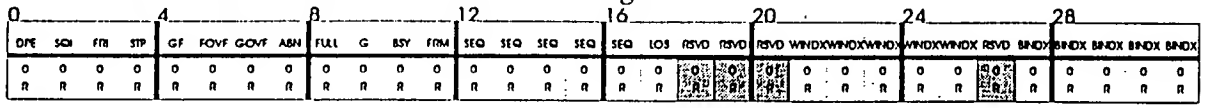
8100 0320 [WO]: ESCON Receiver Control Register



Mnemonic	Size	Description	Notes
CMC	1b	1=Clear Machine Check conditions	
FSt	1b	1=Enable Frame Reception (Clear STOPPED interrupt and conditions)	
CBER	1b	1=Clear BER Condition	
EnG	1b	1=Enable loading G bit	
G	1b	1=Put next incoming frame into G-FIFO 0=Put next incoming frame into FrameStore	
EnBx	1b	1=Enable loading BINDX	
BINDX	5b	Boundary Index (written only when EnBx=1)	

TABLE III

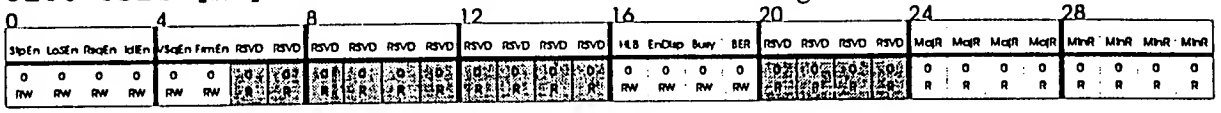
8100 0320 [RO]: ESCON Receiver Status Register



Mnemonic	Size	Description	Notes
DPE	1b	1=CPU Data Parity Error on write (Cleared when RcvCtl/CMC is asserted)	UGLY
SQI	1b	1=Sequence interrupt status (Cleared immediately after RcvStat register is read)	GOOD
FRI	1b	1=Frame interrupt status (Cleared immediately after RcvStat register is read)	GOOD
STP	1b	1=Stopped interrupt status	BAD
GF	1b	1=Receiver G-FIFO Full. This bit is "live" status of the 'Full' flag.	
FOVF	1b	1=Overflow condition detected on FrameStore (causes STP to assert)	BAD
GOVF	1b	1=Overflow condition detected on G-FIFO (causes STP to assert)	BAD
ABN	1b	1=Abnormal condition detected (causes STP to assert)	BAD
FULL	1b	1=FrameStore full. No more frames allowed in FrameStore or G-FIFO because header section of FrameStore is full as defined by BINDX (Cleared on writing RcvCtl/BINDX)	
G	1b	G-bit status	
BSY	1b	1=Receiver Framestore Busy Error	BAD
FRM	1b	1=Frame was received	GOOD
SEQ	5b	Sequence being received on the link: 1xxxx : Rsvd_Seq x1xxx: IDLE 00100: NOS 00101: UD 00110: UDR 00111: OFL	GOOD (Cleared immediately after RcvStat register is read)
LOS	1b	1=LossOfSync (LOS) Detected	
WINDX	5b	Slot number for NEXT received frame	
BINDX	5b	Current Boundary Slot number	

TABLE IV

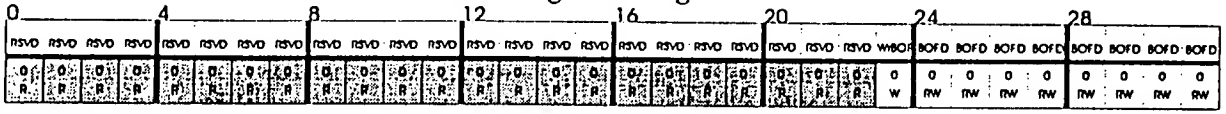
8100 0324 [RW]: ESCON Receiver Mask-Miscellaneous Register



Mnemonic	Size	Description	Notes
StpEn	1b	1=Enable Stop Interrupt	
LoSEn	1b	1=Enable LOS Interrupt	
RsqEn	1b	1=Enable Rsq interrupt	
IdlEn	1b	1=Enable Idle interrupt	
VSqEn	1b	1=Enable VSQ interrupt	
FrmEn	1b	1=Enable Frame interrupt	
HLB	1b	Enable Hotlink Loopback: 1=Receive data from Hotlink Transmitter 0=Receive data from Optical Link	
EnDisp	1b	1=Enable G-FIFO disparity generator	
Busy	1b	1=Software is busy. Instruct hardware to return Link-Busy for connection frames.	
BER	1b	1=Bit-error Violation detected.	Software must write '1' to clear this bit.
MajR	4b	Major Revision of RCVR LCA	Read-Only
MinR	4b	Minor Revision of RCVR LCA	Read-Only

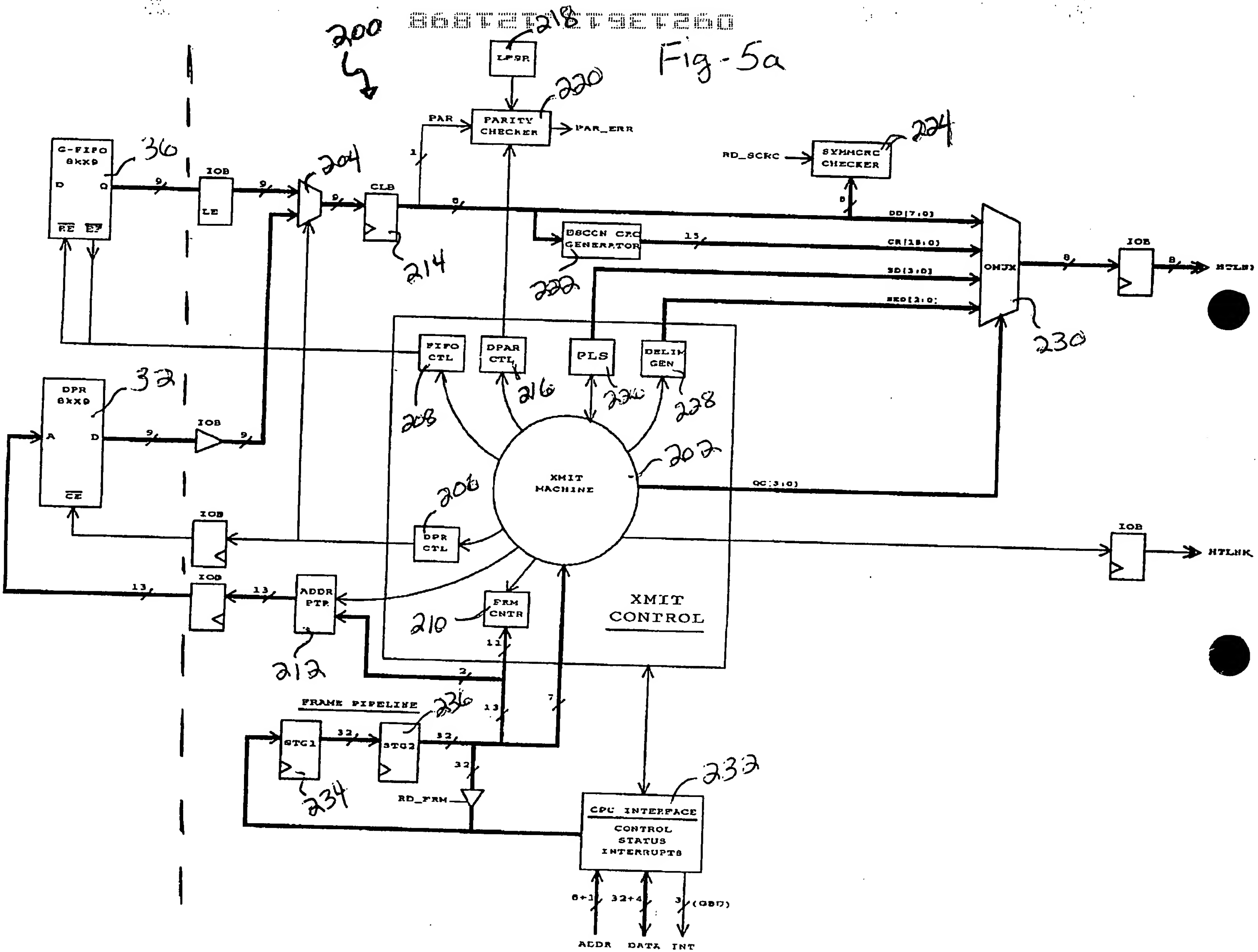
TABLE V

8100 0328 [RW]: ESCON Receive Diagnostic Register



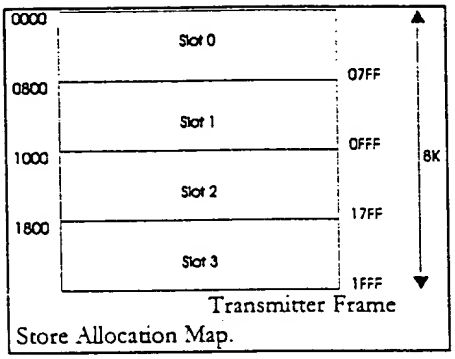
Mnemonic	Size	Description	Notes
WrBOF	1b	1=Execute write operation to incoming G-FIFO	Write-Only
BOFD	8b	Data byte to be written to incoming G-FIFO. Initializes to 00h when RCVR is reset.	

Fig-5a



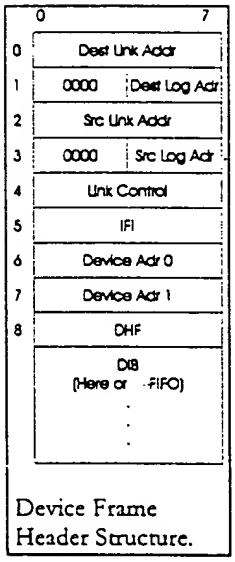
G-FIFO
8KX9
DPR
8KX9
IOB
LE
CLB
PAR
PARITY CHECKER
PAR_ERR
LFSR
SYMMCRC CHECKER
RD_SCRC
DBCCN CRC GENERATOR
DD[7:0]
CR[15:0]
SD[3:0]
SED[2:0]
OMUX
HTLNK
FIFO CTL
DPAR CTL
PLS
DELIM GEN
XMIT MACHINE
QC[3:0]
DPR CTL
ADDR PTR
FRM CNTR
XMIT CONTROL
FRAME PIPELINE
STG1
STG2
RD_FRM
CPU INTERFACE
CONTROL
STATUS
INTERRUPTS
ADDR
DATA
INT

Fig 5b

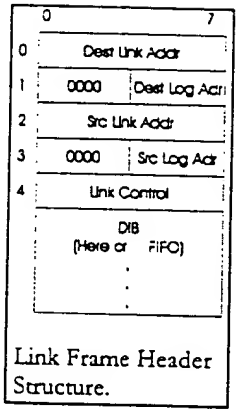


Transmitter Frame Store Allocation Map.

Fig 5d



Device Frame Header Structure.

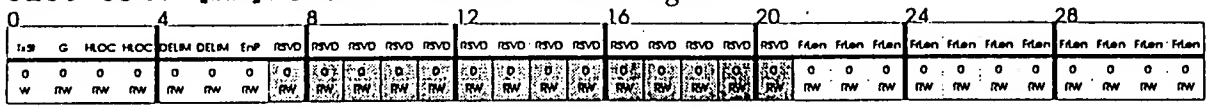


Link Frame Header Structure.

Fig. 5c

TABLE VI

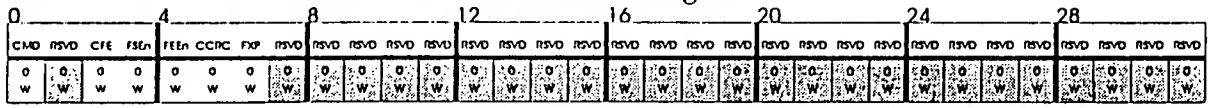
8100 0340 [RW]: ESCON Transmitter Frame Register



Mnemonic	Size	Description	Notes
TxSt	1b	1=Start frame transmission	Write-Only
G	1b	Location of Frame DIB: 0=DIB in Frame Store 1=DIB in G-FIFO	Link frames should have bit clear; Device frames can have either clear/set
HLOC	2b	Location of Frame Header	
DELIM	2b	Frame Delimiters: 00=PSOF, PEOF 01=CSOF, PEOF 10=PSOF, DEOF 11=Not Defined	
EnP	1b	1=Enable Pacing (pacing bytes are appended to end of this frame)	
FrLen	11b	Frame Length (Header + DIB)	

TABLE VII

8100 0344 [WO]: ESCON Transmitter Control Register



Mnemonic	Size	Description	Notes
CMC	1b	1=Clear Machine Check conditions	
CFE	1b	1=Clear Frame-Error interrupt and conditions	
FSEn	1b	1=Enable Frame-Sent interrupt	
FEEn	1b	1=Enable Frame-Error interrupt	
CCRC	1b	1=Clear the Xmit G-FIFO Symmetrix CRC	
FXP	1b	1=Flush the entire Xmit pipeline	

TABLE VIII

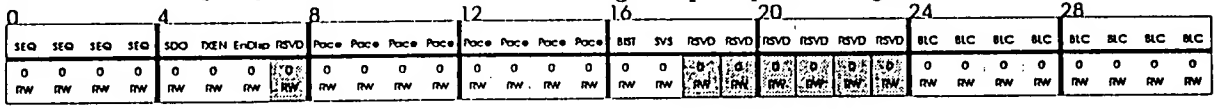
8100 0344 [RO]: ESCON Transmitter Status Register

0				4				8				12				16				20				24				28			
DPE	FS	FE	FSEn	FEEn	GMT	OVF	GPE	FPE	IW	IRQ	XPF	XPE	GE	BSY	RSVD	GCRC	GCRC	GCRC	GCRC	GCRC	GCRC	GCRC	GCRC	MajR	MajR	MajR	MajR	MinR	MinR	MinR	MinR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Mnemonic	Size	Description	Notes
DPE	1b	1=CPU Data Parity Error on Write (Cleared when XmtCtl/CMC is asserted)	UGLY
FS	1b	Frame-Sent status	GOOD
FE	1b	Frame-Error status	BAD
FSEn	1b	1=Frame-Sent interrupt enabled	
FEEn	1b	1=Frame-Error interrupt enabled	
GMT	1b	1=Xmit G-FIFO Empty (while sending frame)	BAD
OVF	1b	1=Frame Overflow (Frame > 1035 bytes)	BAD
GPE	1b	1=Xmit G-FIFO Parity Error	BAD
FPE	1b	1=Xmit FrameStore Parity Error	BAD
IW	1b	1=Illegal Write	BAD
IRQ	1b	1=Illegal Request	BAD
XPF	1b	1=Xmit Pipe Full	
XPE	1b	1=Xmit Pipe Empty	
GE	1b	1=Xmit G-FIFO Empty	live status/empty flag
BSY	1b	1=Xmit Framestore Busy Error	BAD
GCRC	8b	Xmit G-FIFO Symmetrix CRC	
MajR	4b	Major Revision of XMIT LCA	
MinR	4b	Minor Revision of XMIT LCA	

TABLE IX

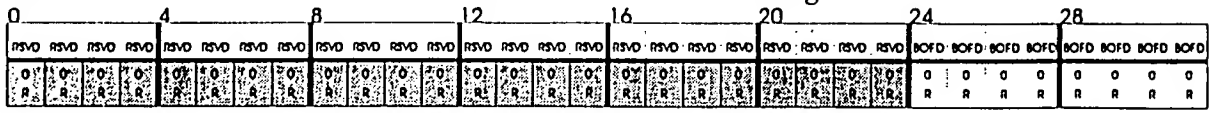
8100 0348 [RW]: ESCON Transmitter Pacing-Loop-Sequence Register



Mnemonic	Size	Description	Notes
SEQ	4b	Sequence Identifier 1111: Offline 1001: Not Operational 1011: UD 1101: UDR xxx0: Idle 0xx1: Reserved	
SDO	1b	1=Enable Pseudo Frame condition	
TXEN	1b	0=Enable Fiber-Optic Transmitter	Active-Low
EnDisp	1b	1=Enable Xmit G-FIFO disparity checker	
Pace	8b	Pacing Count - 1's complement	
BIST	1b	0=Enable Hotlink Built-In Self-Test (diagnostic)	not yet implemented
SVS	1b	1=Send Violation Sequence (diagnostic)	not yet implemented
BLC	8b	BIST Loop Counter (diagnostic)	not yet implemented

TABLE X

8100 034C [RO]: ESCON Transmitter Bottom-Of-FIFO Register



Mnemonic	Size	Description	Notes
BOFD	8b	Data byte read from outgoing G-FIFO	Read-Only

Fig-6

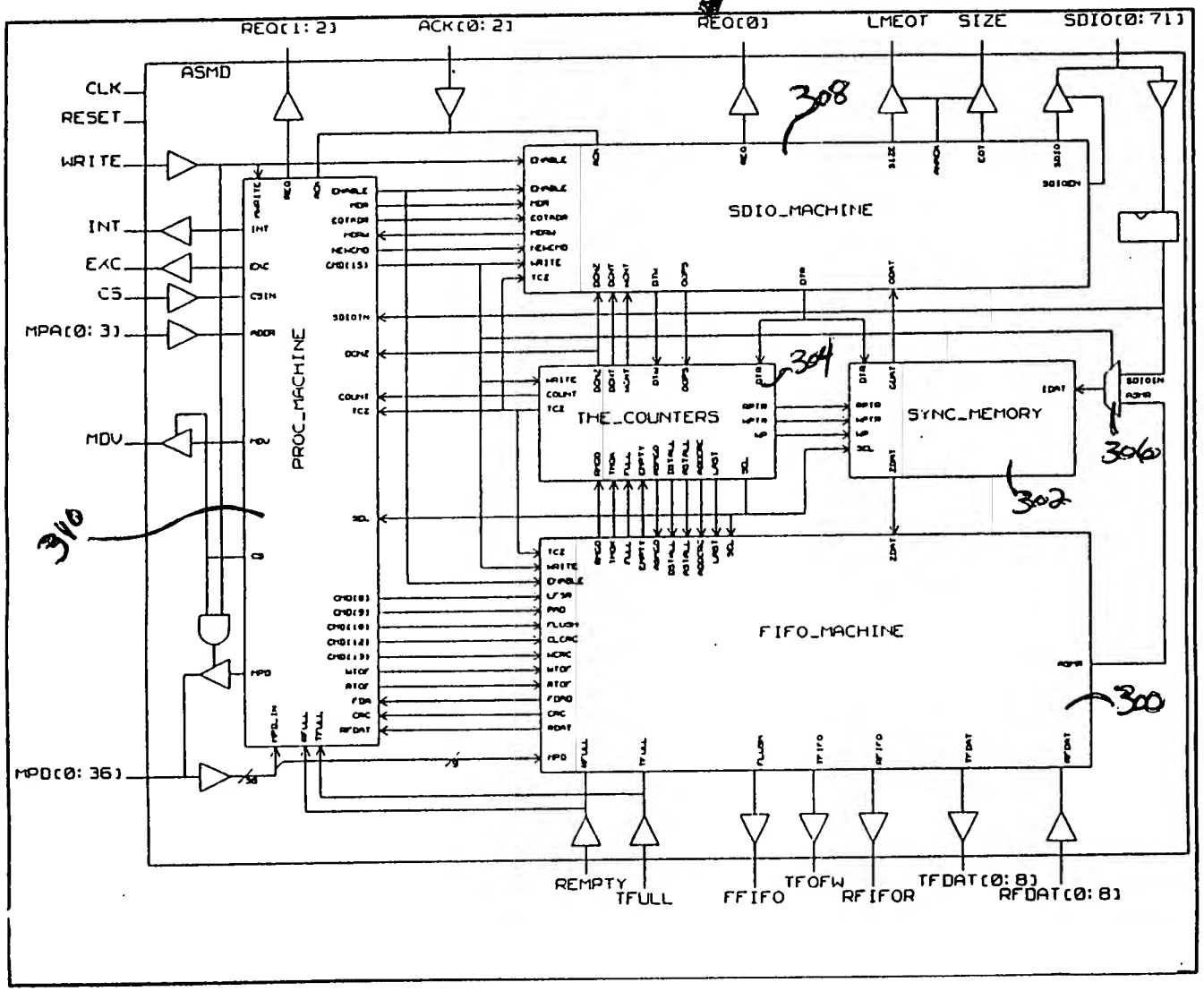
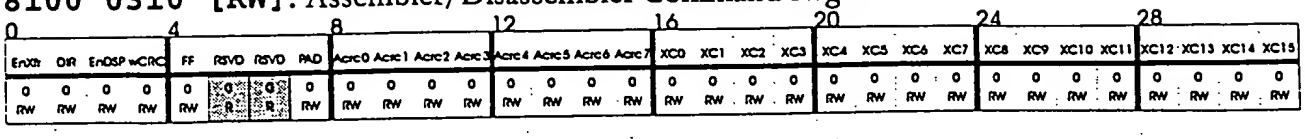


TABLE XI

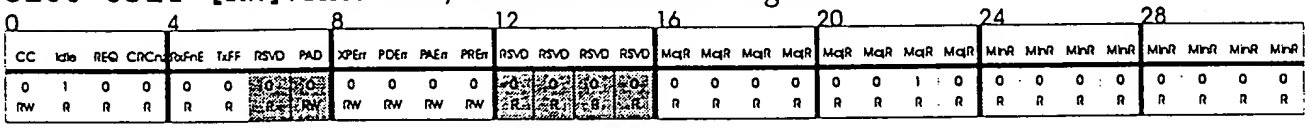
8100 0310 [RW]: Assembler/Disassembler Command Register



Mnemonic	Size	Description	Notes
EnXfr	1b	1=Enable Transfer	
DIR	1b	1=Write (Line to DPR) 0=Read (DPR to Line)	
EnDSP	1b	1=Enable disparity generator	
wCRC	1b	1=Enable appending CRC to end of data	
FF	1b	1=Flush FIFO	
PAD	1b	1=Enable 0 padding through ADT pipe	
Acrc0-Acrc7	8b	Accumulated CRC for current transfer	
XC0-XC15	16b	Number of bytes to transfer	Readback gives # of bytes remaining to transfer

TABLE XII

8100 0314 [RW]: Assembler/Disassembler Status Register



Mnemonic	Size	Description	Notes
CC	1b	1=Machine is Idle	
REQ	1b	1=ADT Request Outstanding to Middle Machine	*H/W diagnostic use*
PFErr	1b	1=Parity Error in SCSI transfer	BAD
Pderr	1b	1=Processor Data Bus Parity Error detected	BAD
Paerr	1b	1=Processor Address Bus Parity Error detected	BAD
CRCErr	1b	1=CRC not zero	
Acrc0-Acrc7	8b	Accumulated CRC for current transfer	
CC0-CC15	16b	Current transfer count	

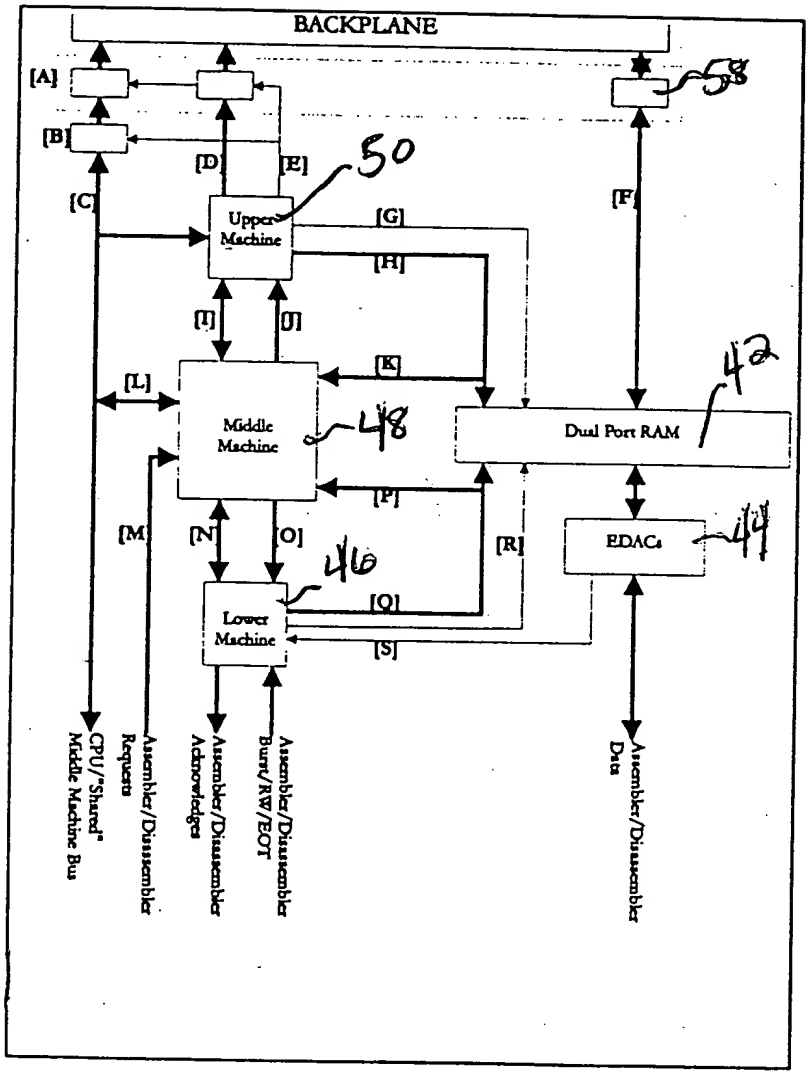

BACKPLANE
[A]
[B]
[C]
[D]
[E]
50
Upper Machine
[F]
58
[G]
[H]
[I]
[J]
[K]
[L]
Middle Machine
48
Dual Port RAM
42
[P]
[M]
[N]
[O]
46
[R]
EDACs
44
[Q]
Lower Machine
[S]
CPU/"Shared" Middle Machine Bus
Assembler/Disassembler Requests
Assembler/Disassembler Acknowledges
Assembler/Disassembler Burst/RW/EOT
Assembler/Disassembler Data

Fig-7

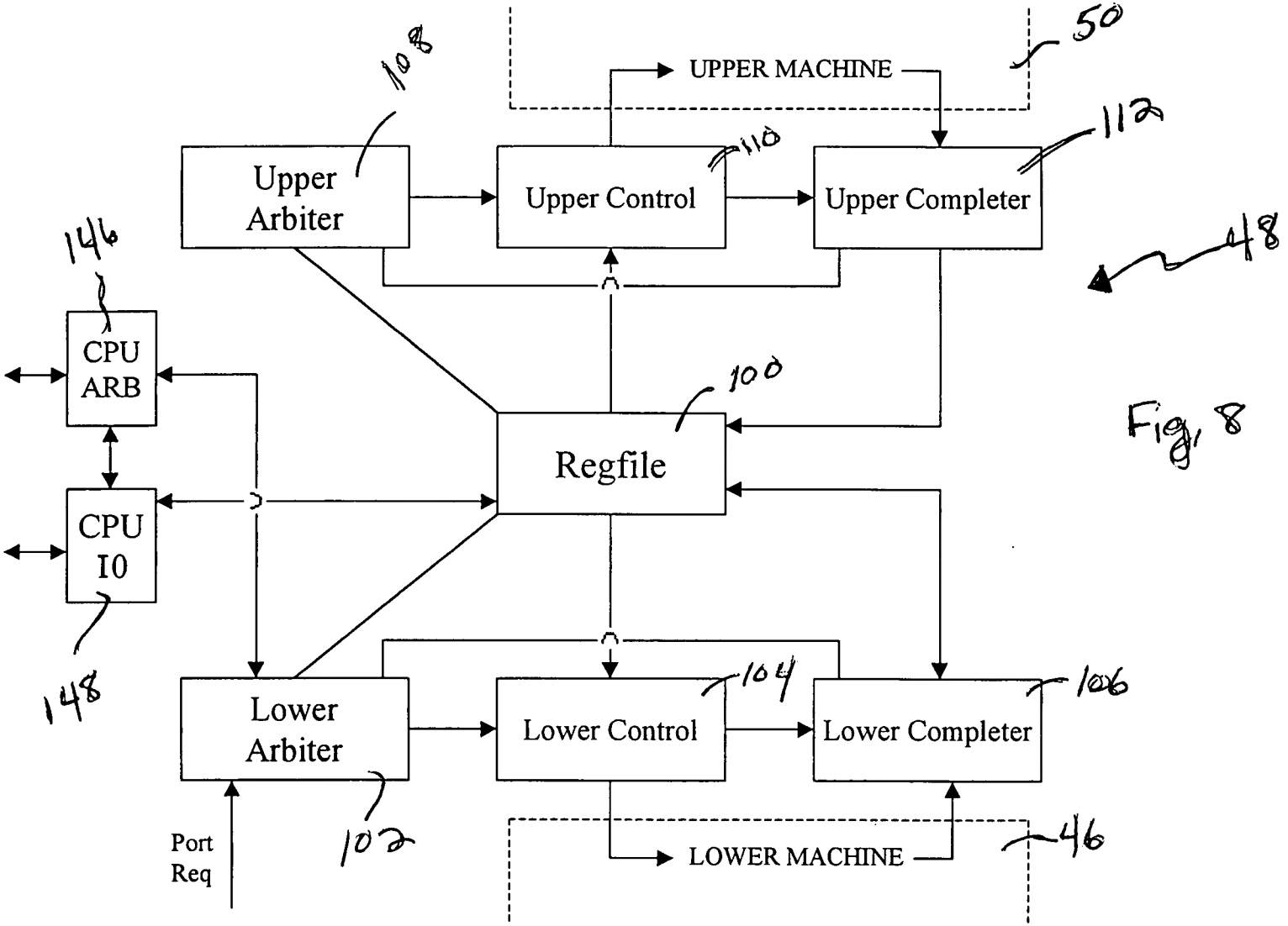
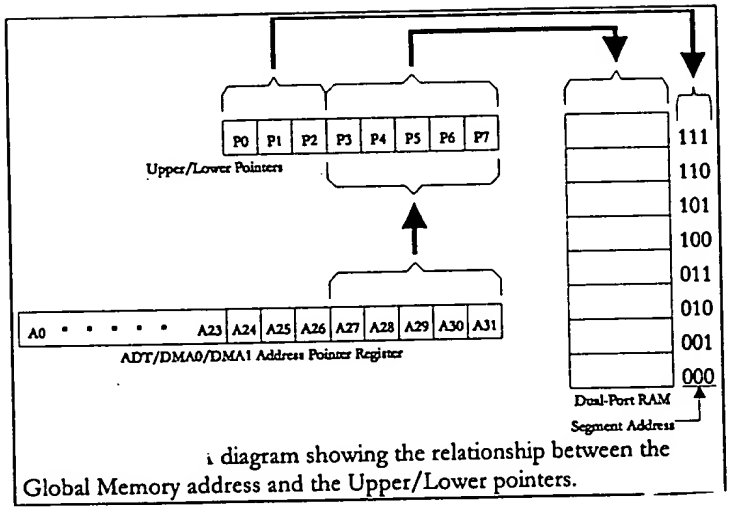
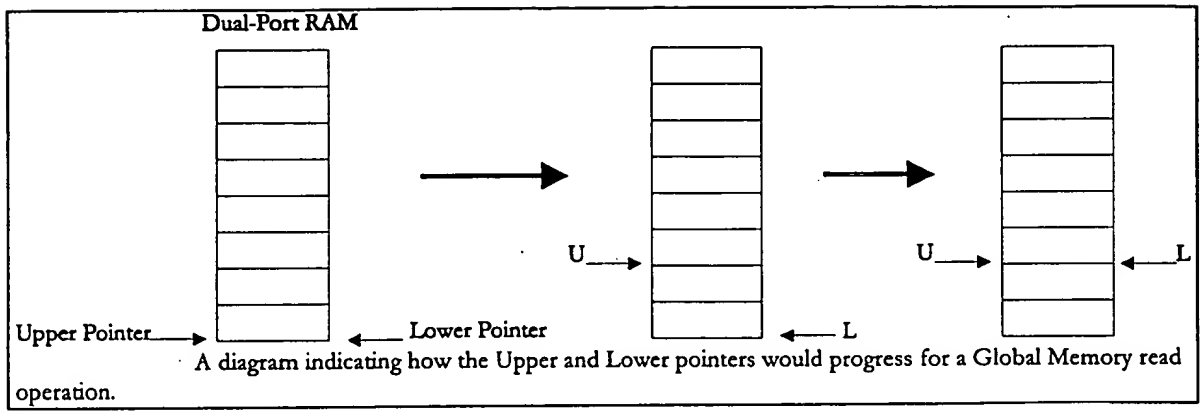


Fig. 8



a diagram showing the relationship between the Global Memory address and the Upper/Lower pointers.

Fig. 9

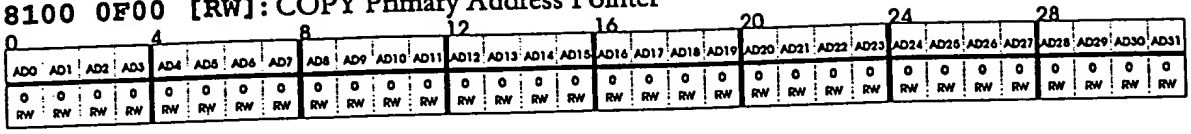


A diagram indicating how the Upper and Lower pointers would progress for a Global Memory read operation.

Fig-10

TABLE XIII

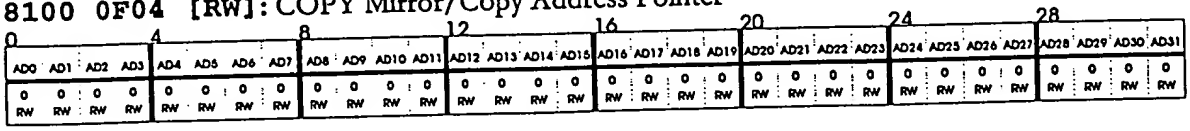
8100 0300 [RW]: ADT Primary Address Pointer
8100 0700 [RW]: DMA0 Primary Address Pointer
8100 0B00 [RW]: DMA1 Primary Address Pointer
8100 0F00 [RW]: COPY Primary Address Pointer



Mnemonic	Size	Description	Notes
AD0-AD31	32b	Primary Global Memory DWord Address, or Source Address for COPY operation	

TABLE XIV

8100 0304 [RW]: ADT Mirror/Copy Address Pointer
8100 0704 [RW]: DMA0 Mirror/Copy Address Pointer
8100 0B04 [RW]: DMA1 Mirror/Copy Address Pointer
8100 0F04 [RW]: COPY Mirror/Copy Address Pointer



Mnemonic	Size	Description	Notes
AD0-AD31	32b	Mirror Global Memory DWord Address for Mirror Write Operations, or Destination Address for COPY operation	

TABLE XV

8100 0308 [RW]: ADT Command & Transfer Length Register
8100 0708 [RW]: DMA0 Command & Transfer Length Register
8100 0B08 [RW]: DMA1 Command & Transfer Length Register
8100 0F08 [RW]: COPY Command & Transfer Length Register

0				4				8				12			
RSVD	RSVD	TL0	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	TL13
[illegible]	[illegible]	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW

16				20				24				28			
RSVD	RSVD	MIR	COPY	FP	IEC	FE	EOT	RSVD	RW	XOR	SVC	LOCK	RSVD	SPAR	EC
[illegible]	[illegible]	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	[illegible]	0 RW	0 RW	0 RW	0 RW	[illegible]	0 RW	0 RW

Mnemonic	Size	Description	Notes
TL0-TL13	14b	Number of DWords to read or write	
MIR	1b	1=Mirror all Global Memory writes to the Mirror Address given in the Mirror Address Pointer	
COPY	1b	1=Perform a true DMA operation; Reads occur from the primary Address Pointer, Writes are destined for the Copy Address Pointer; Transfer length is given by TL0-13.	RW must be set; SVC&MIR are illegal; XOR may be used
FP	1b	Middle Machine First Pass internal arbiter bit	Must be set to '1'
IEC	1b	Middle Machine Internal Enable Channel	Must be set to '1'
FE	1b	1=Fatal Error Occurred During Transfer	
EOT	1b	1=End Of Transfer has occurred 1=Force End Of Transfer protocol in Middle Machine	When Read When Written
RW	1b	1=Read 0=Write	
XOR	1b	1=XOR the new data with the current data in Global Memory, then store the result in Global Memory	Only valid for Writes with or without Mirror
SVC	1b	1=Backplane cycles will be initiated as Service Cycles	
LOCK	1b	1=Lock Memory	
RSVD	1b	Reserved Command bit	Must be set to '0'
SPAR	1b	Backplane SPARE bit	Must be set to '0'
EC	1b	1=Enable Channel 0=Disable Channel	An interrupt will be generated after the Middle Machine completes current pass

TABLE XVI

8100 030C [RW]: ADT Status/Upper & Lower Pointers
8100 070C [RW]: DMA0 Status/Upper & Lower Pointers
8100 0B0C [RW]: DMA1 Status/Upper & Lower Pointers
8100 0F0C [RW]: COPY Status/Upper & Lower Pointers

0				4				8				12				16				20				24				28			
ERR	CTMS	ETNZ	UEC0	UEC1	MPE	RSVD	INITS	CC0	CC1	CC2	CC3	LEC0	LEC1	LEC2	DMC	UP0	UP1	UP2	UP3	UP4	UP5	UP6	UP7	LP0	LP1	LP2	LP3	LP4	LP5	LP6	LP7
0 RW	0 RW	0 RW	0 RW	0 RW	0 RW		0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW	0 RW

Mnemonic	Size	Description	Notes
ERR	1b	1=An Error Occurred during the transfer	
CTMS	1b	1=Count Miss occurred	
ETNZ	1b	1=Ending Transfer Count Not Zero error occurred	
UEC0-1	2b	Upper Error Codes	See table below
MPE	1b	1=Machine Parity Error occurred (CPU Parity Error / Internal Parity Error)	
INITS	1b	1=Global Memory reported Initial Status	
CC0-CC3	4b	Ending Global Memory Condition Codes	0101=good status
LEC0-2	3b	Lower Error Codes	See table below
DMC	1b	1=DMA Operation Completed	
UP0-UP7	8b	Upper Machine DPR Pointer	
LP0-LP7	8b	Lower Machine DPR Pointer	

M0/M1 Condition Codes:

Condition Code	Meaning	Notes
0101 (5)	Good Ending Status (No Errors)	
1001 (9)	Protocol Error	
1110 (E)	Count Miss	
1000 (8)	R/W Mismatch	
1010 (A)	Multi-bit Error	
0011 (3)	Single-bit Error	
0111 (7)	Memory Internal Error	
1101 (D)	More Than One Ending Status Error	

Upper Error Codes:

Code	Meaning
00 (0)	No Upper Machine Hardware Errors
01 (1)	Short Timeout Occurred
10 (2)	Long Timeout Occurred
11 (3)	Lock Timeout or Upper Machine Command Parity Error Occurred

Lower Error Codes:

Code	Meaning
000 (0)	No Lower Machine Hardware Errors
001 (1)	Single-Bit EDAC Error Detected
010 (2)	Reserved
011 (3)	Multi-Bit EDAC Error Detected
100 (4)	Parity Error detected on SDIO bus
101 (5)	Reserved
110 (6)	Illegal Lower Machine/ASMD Transfer Size Detected
111 (7)	ASMD Lower Machine Command Parity Error

Lower Arbiter

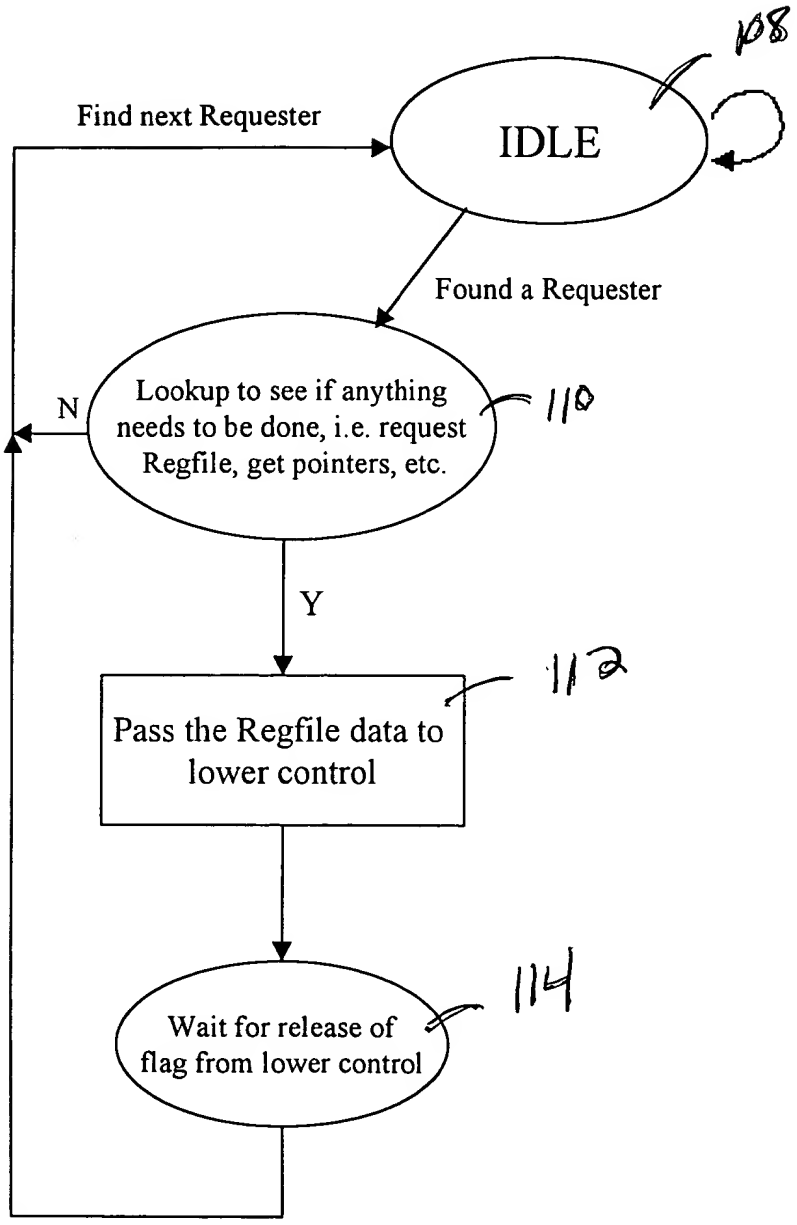


Fig. 11

Lower Control

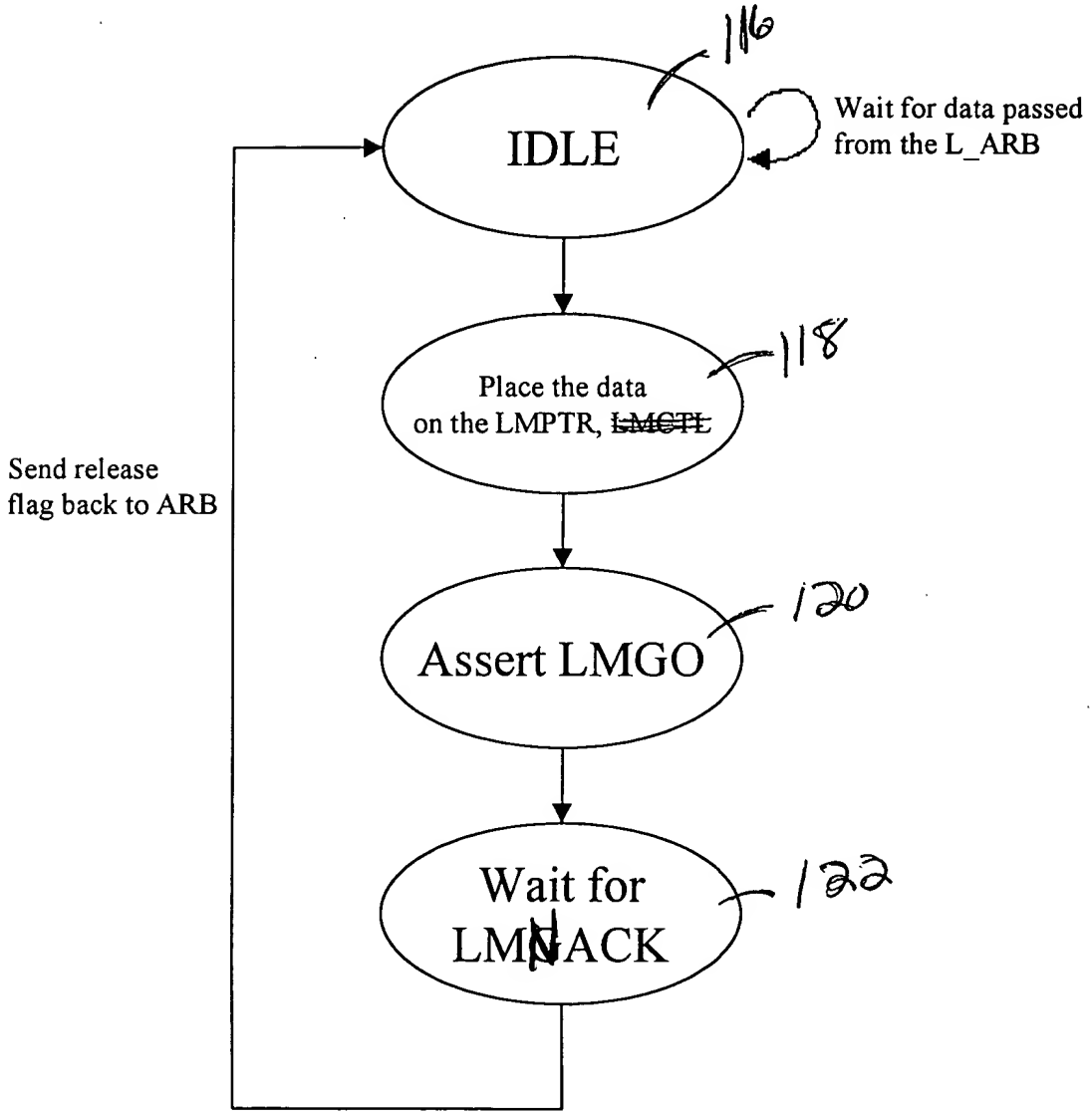


Fig - 12

Lower Completer

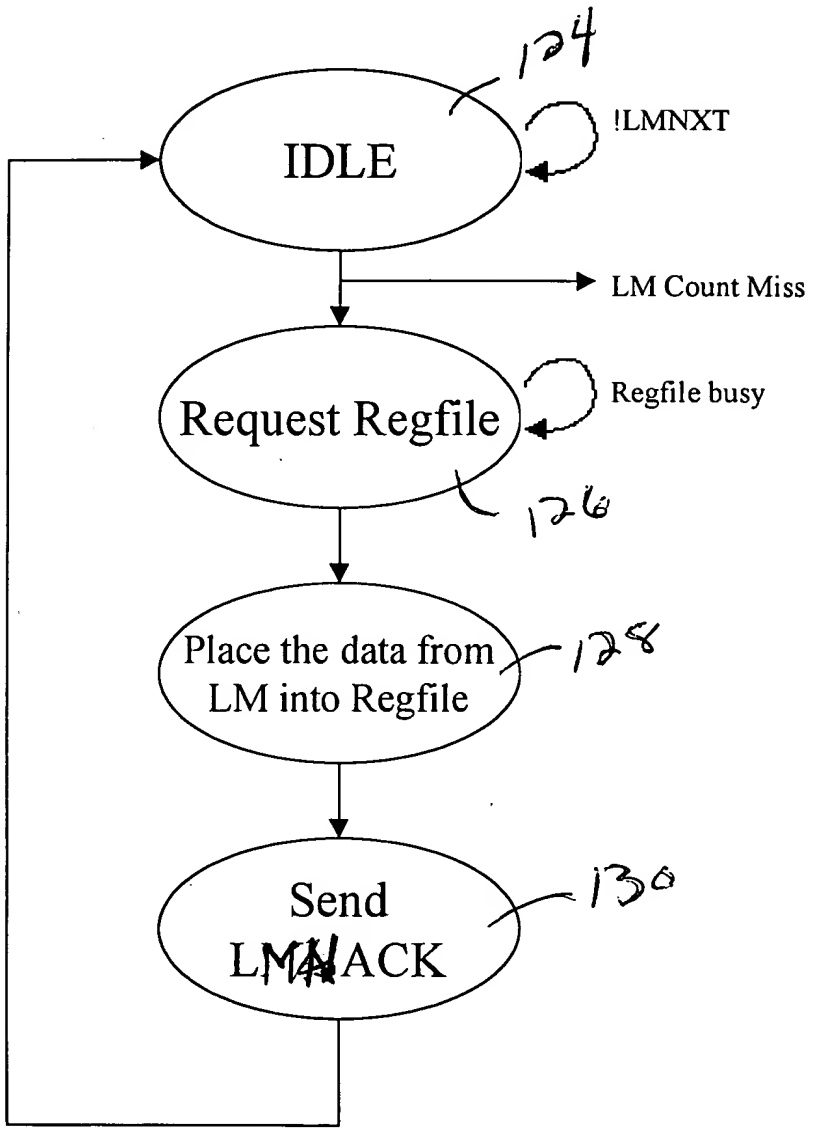


Fig. 13

Upper Arbiter

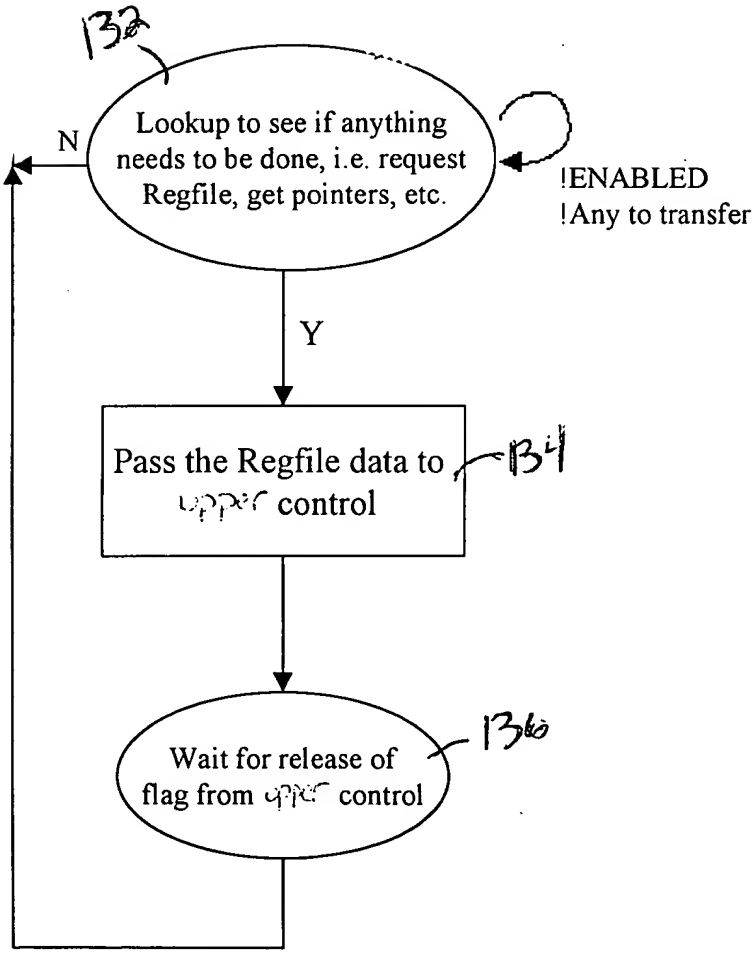


Fig. 14

Upper Control

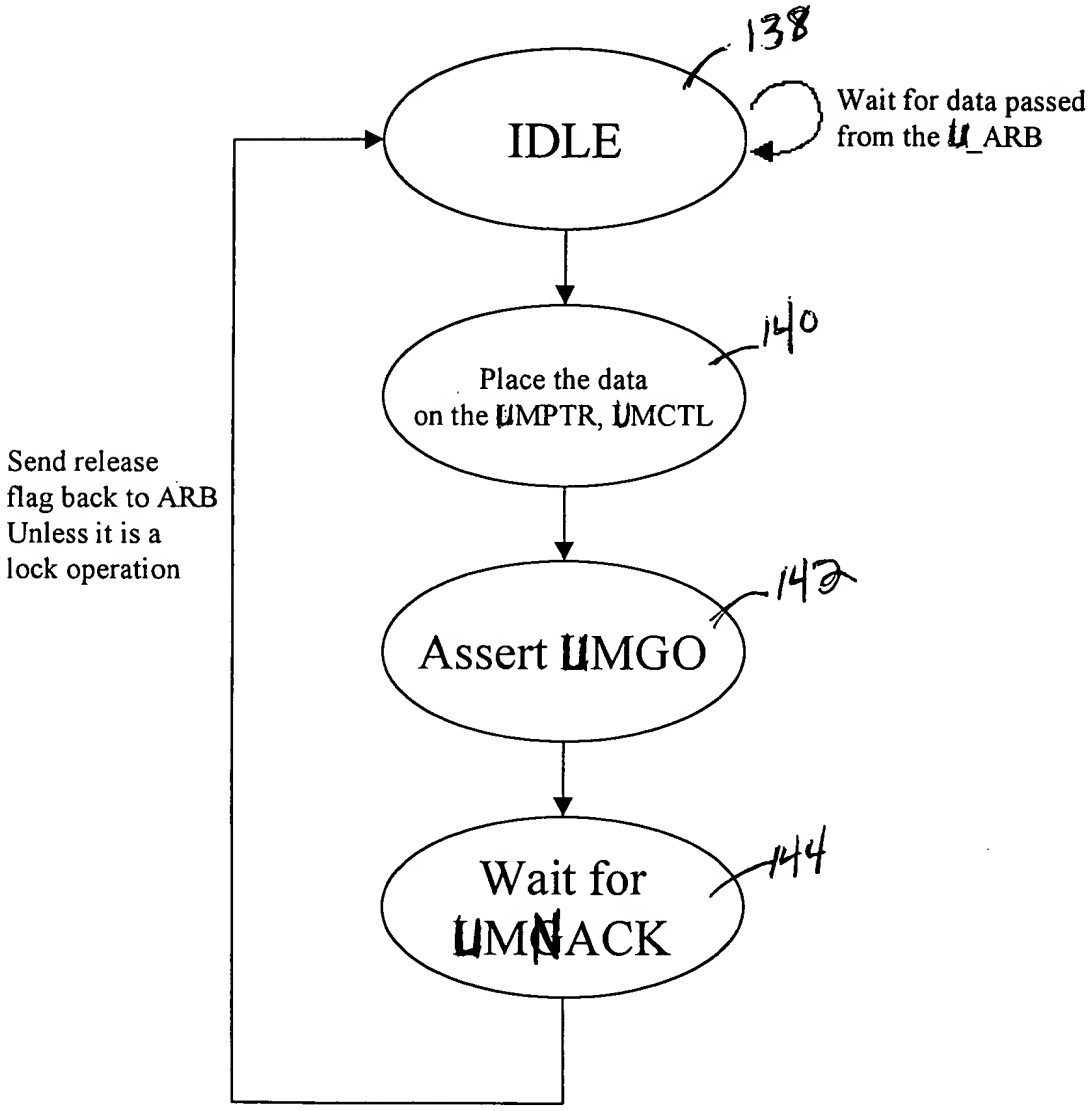


Fig. 15

Upper Completer

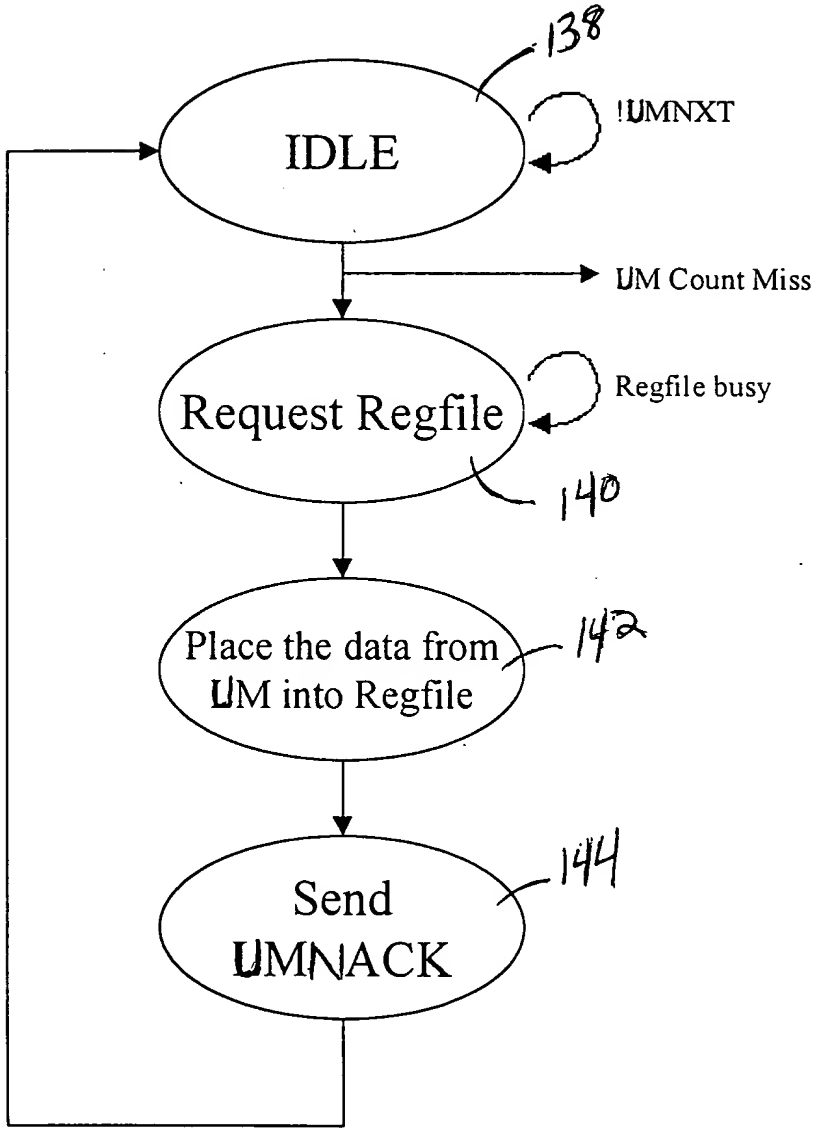


Fig. 16

Fig. 17